Exploration of Fault Effects on Formal RISC-V Microarchitecture Models

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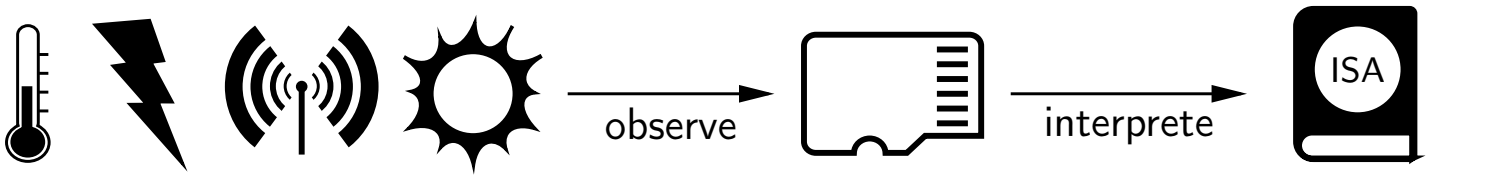
FDTC, September 16, 2022

Fault Effects Characterization

Experimental characterization



Most common observed effects

- Instruction skips [Riviere, 2015] [Menu, 2020]
- Instruction replacement [Moro, 2013] [Trouchkine, 2020]
- Data corruption

Microarchitectural Fault Effects

Recent work

- Some effects cannot be *explained* at the ISA level
  - *Magic edges* [Proy, 2019]
- Some effects cannot be *captured* at the ISA level
  - *Forwarding* [Laurent, 2018]

ISA-level fault effect modeling

- Encompass broad set of effects
- Convenient for software analysis
- Abstract the implementation details

➔ Not sufficient to fully understand potential of fault injection

Contribution

Automated formal modeling of HW and SW

➔ For exploring microarchitectural fault effects on SW security

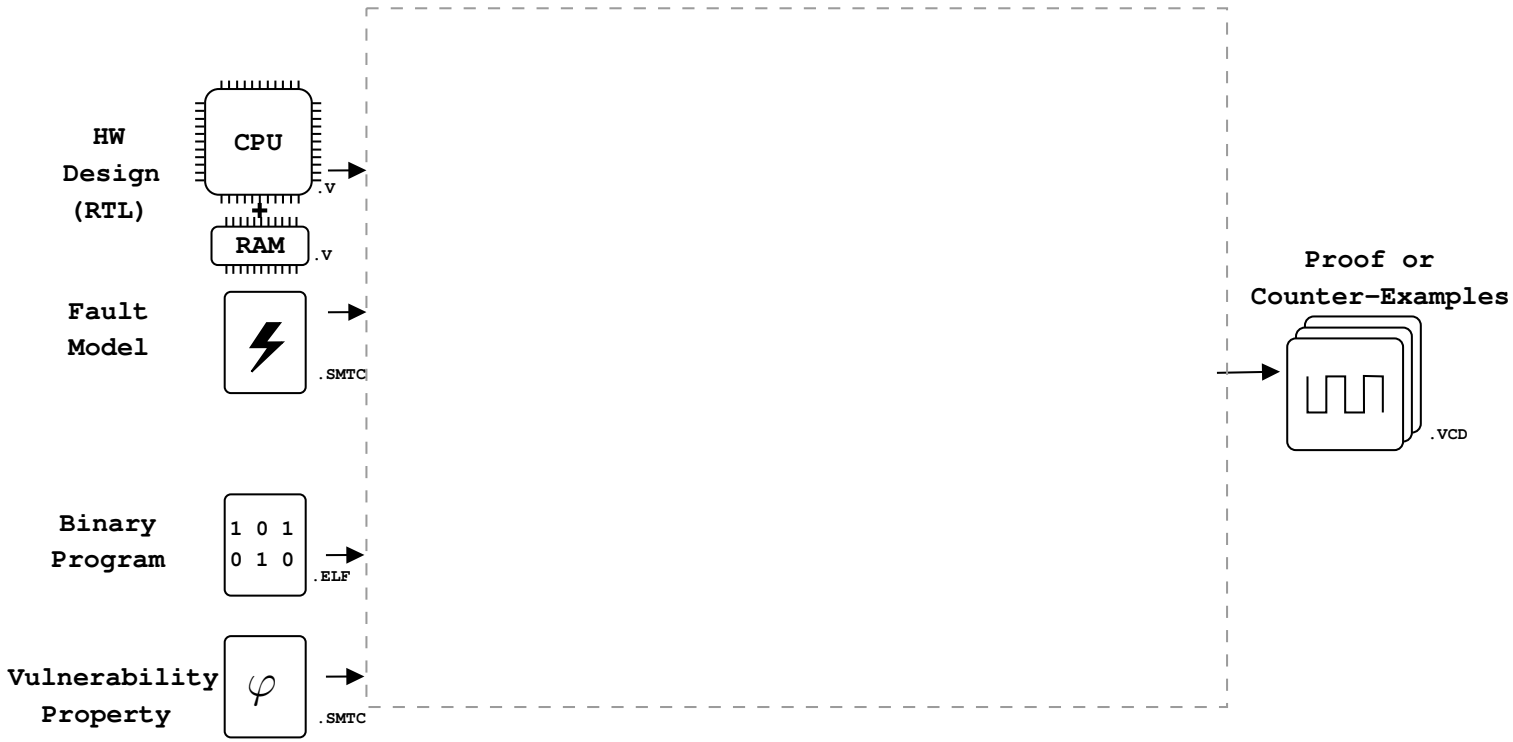
➔ For analyzing the robustness of HW or SW countermeasures

Why using formal methods, e.g., model checking?

- Give counterexamples or a proof
- Verification process guided toward counter-examples
- Handle complex properties in various logics

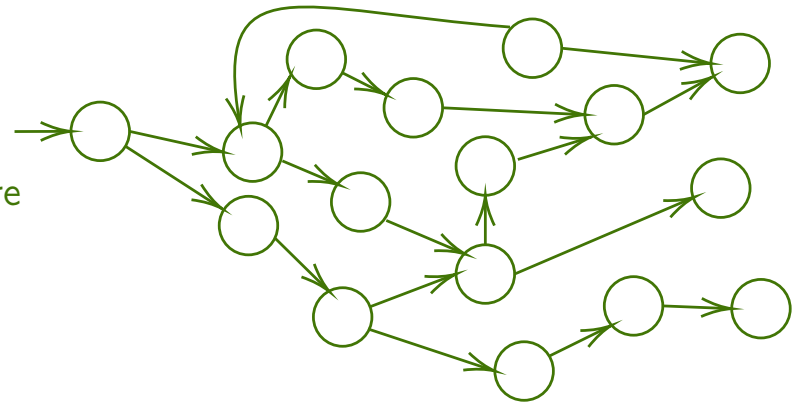
Workflow: Modeling Steps

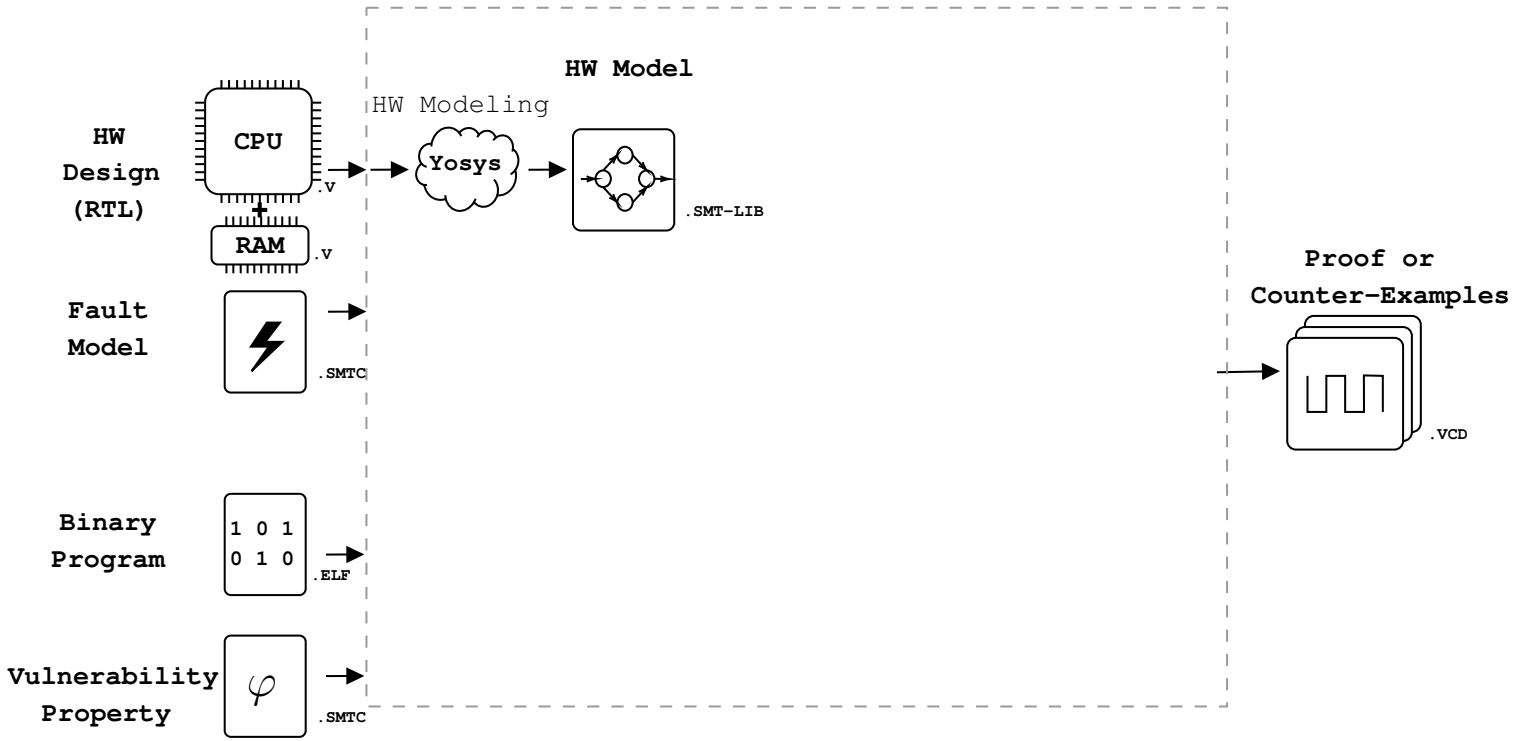
Inputs / Outputs



Workflow: Modeling Steps

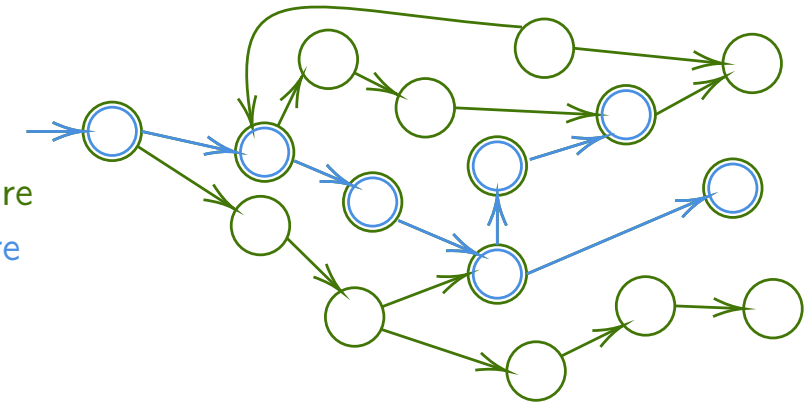
Hardware Modeling



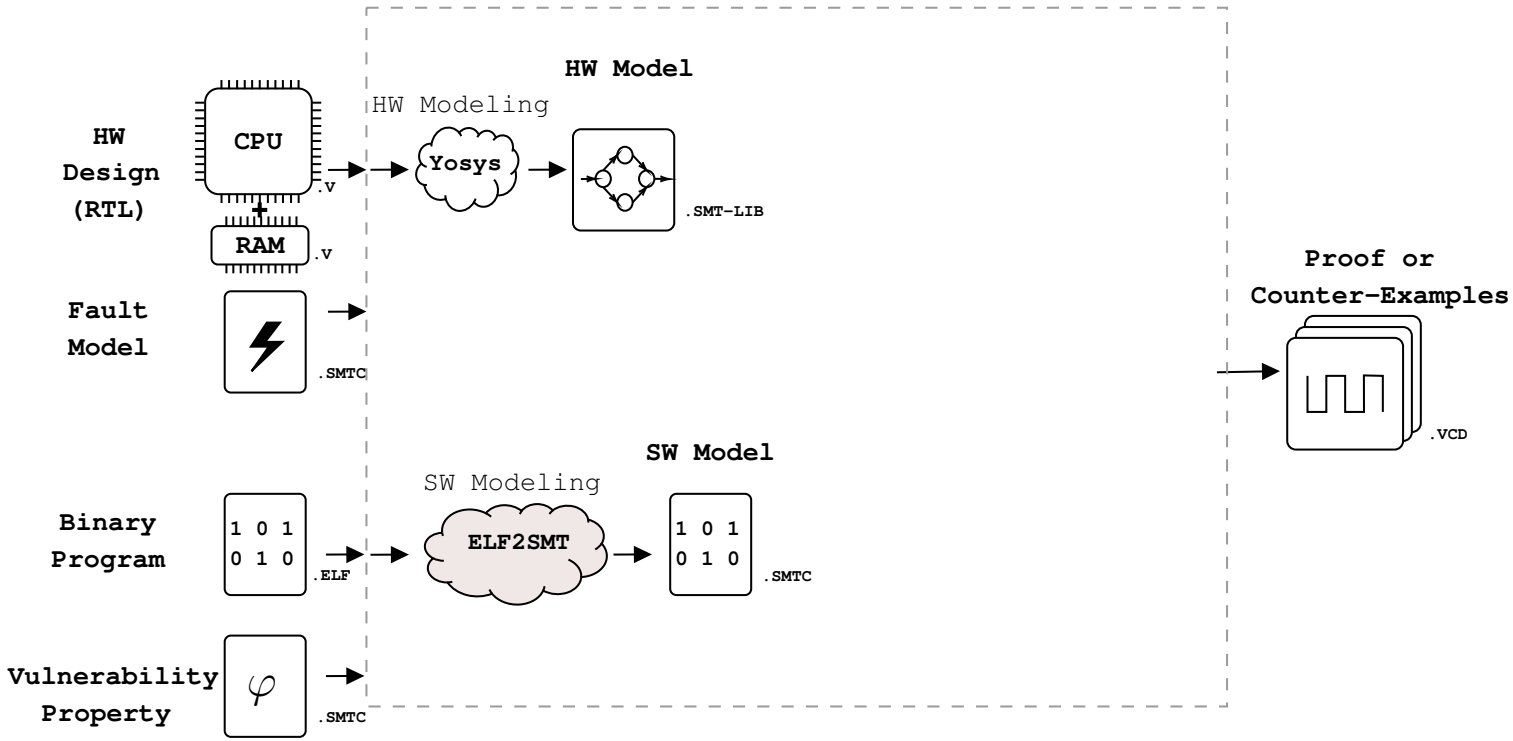


Workflow: Modeling Steps

Software Modeling

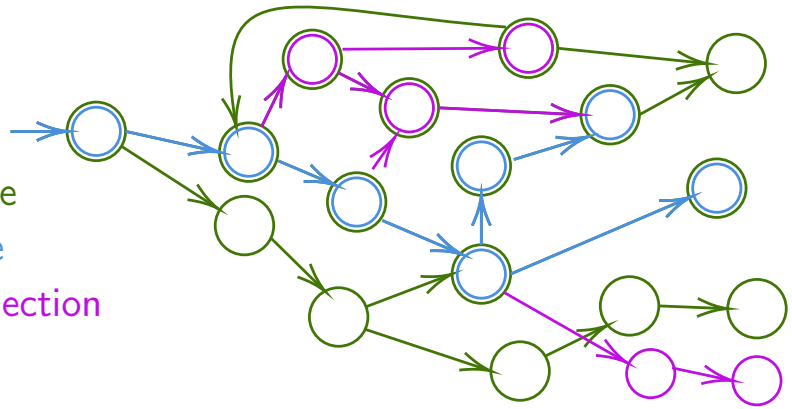


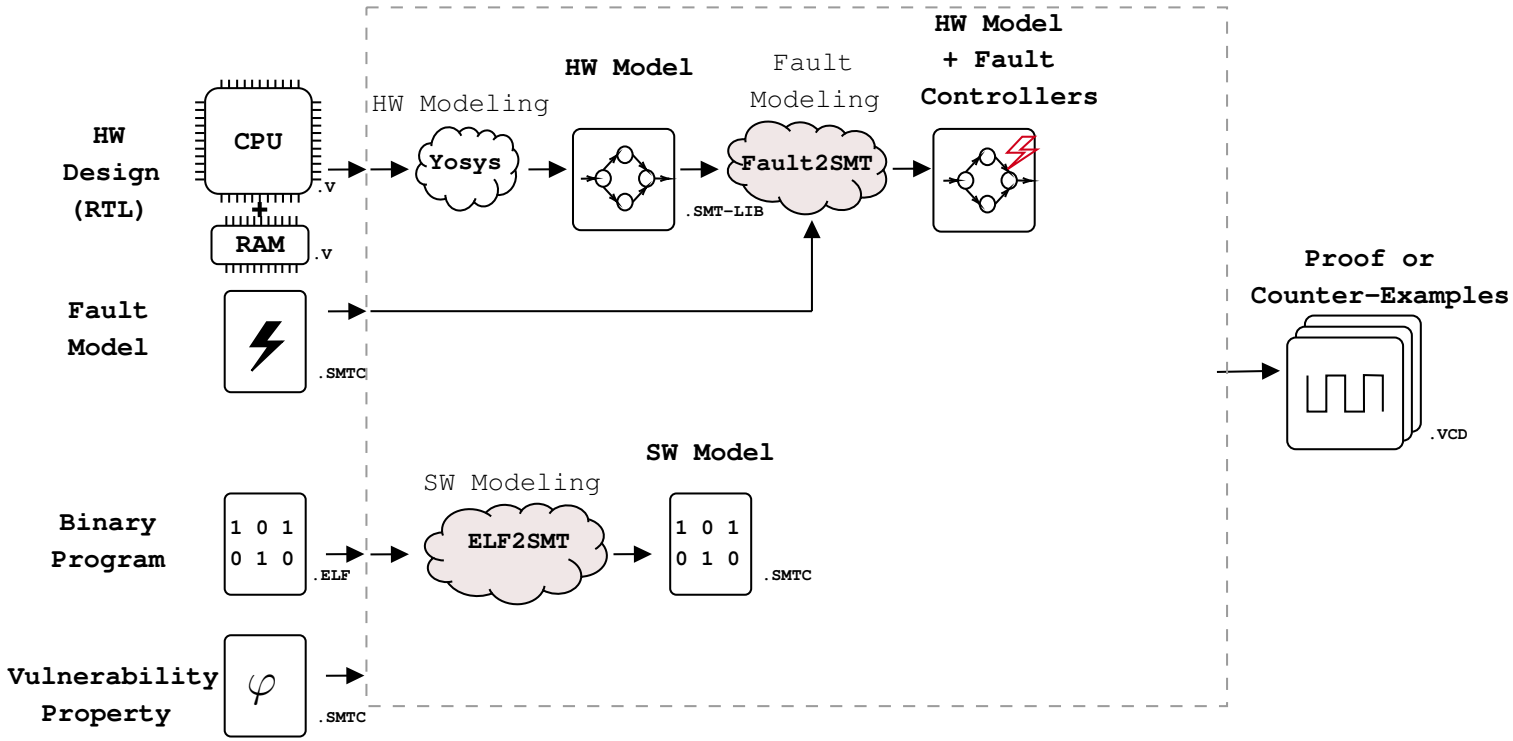
— Hardware
— Software



Workflow: Modeling Steps

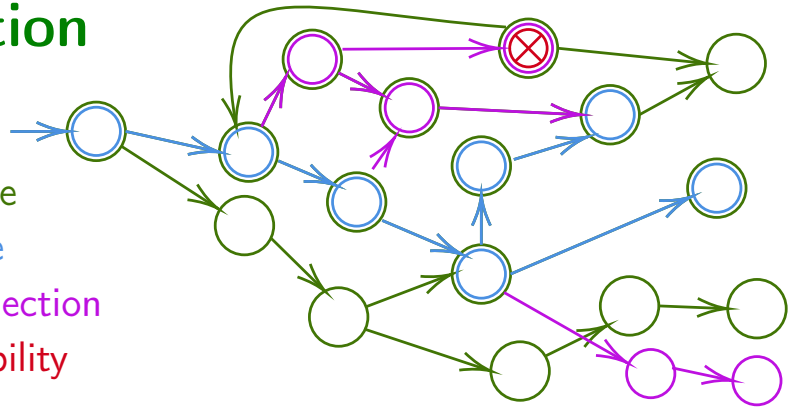
Fault Modeling



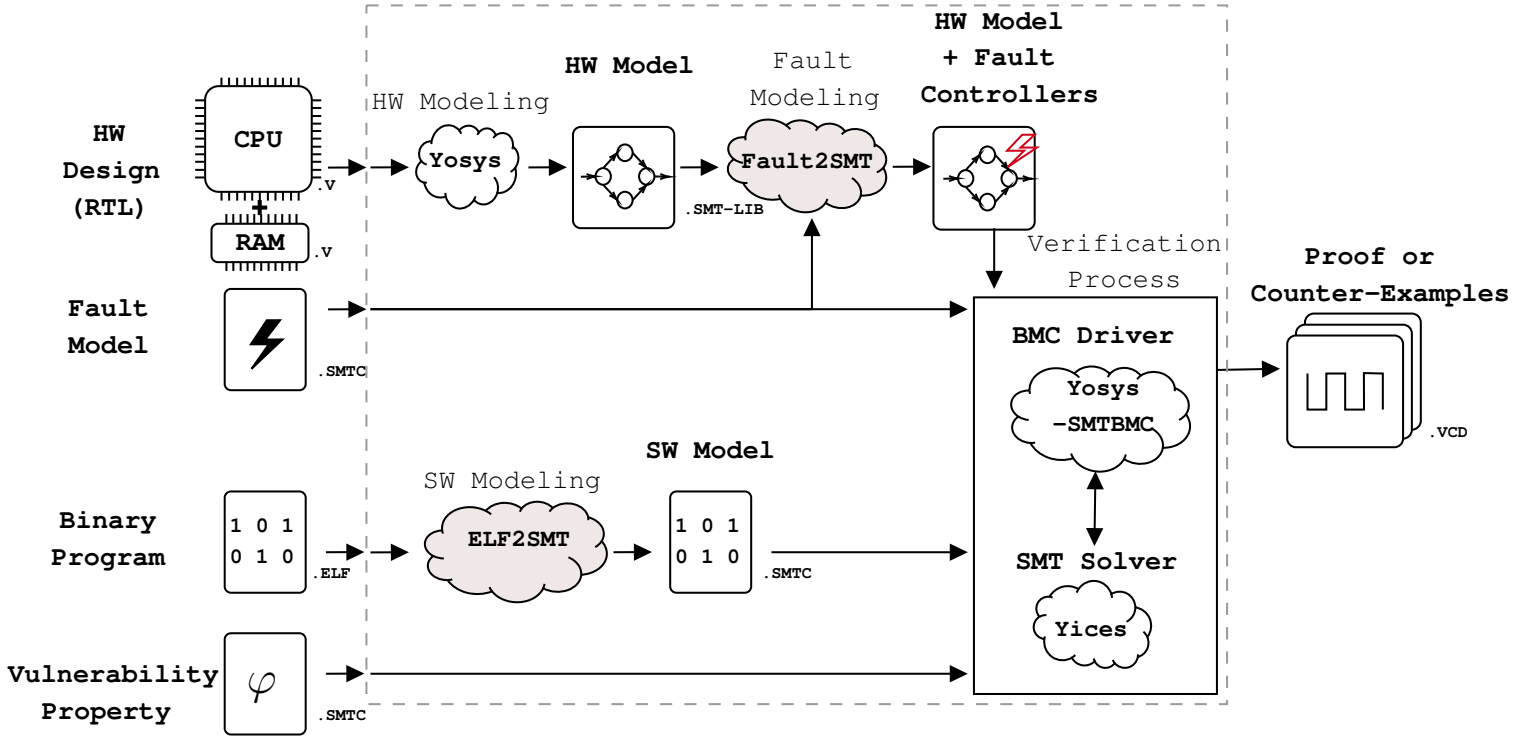


Workflow: Modeling Steps

Property Specification

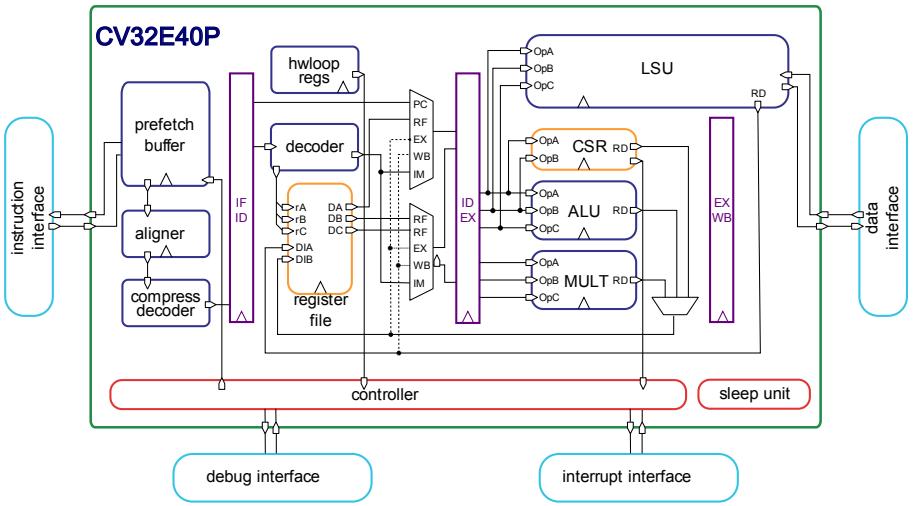


— Hardware
— Software
— Fault Injection
— Vulnerability



Hardware Part

CV32E40P



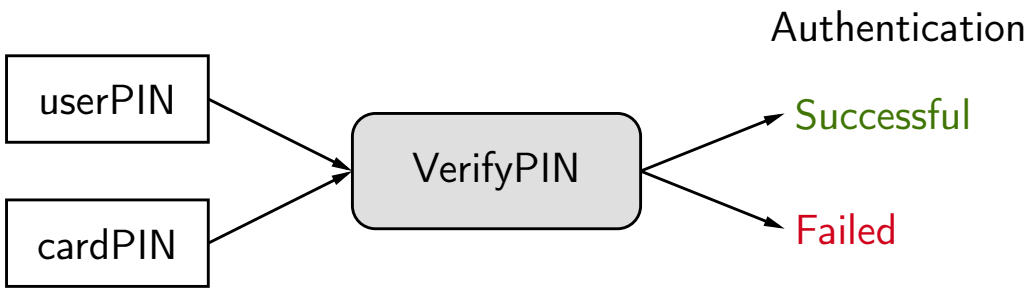
- Standard version [CV32E40P]
- Hardened version [Chamelot, 2022]
  - Control flow integrity
  - Code integrity
  - Execution integrity

Microarchitectural Fault Model

- Single fault injection
- During the whole program
- Everywhere in the circuit
- Symbolic fault effect

Software Part

VerifyPIN




```
Compare {
   for ( i = 0 ; i < 4 ; i ++) {
      if(userPIN[i] != cardPIN[i])
         return false;
   return true;
}

VerifyPIN {
   authentification = false;
   if (tries > 0) {
      if(Compare()) {
         tries = 3 ;
         authentification = true;
      } else {
         tries -- ;
      }
   }
}
```

- Standard version [Dureuil, 2016]
- Versions implementing SW countermeasures
  - Constant iteration number loop
  - Inline function calls
  - Duplication of critical tests

Security Property

- $\texttt{userPIN} \neq \texttt{cardPIN} \implies$ Authentication is not possible

Countermeasures have attack oracles to detect fault injections

Fault Effects Exploration Results

Find known attacks

- Exploiting the forwarding mechanism

Find new fault effects

- **Immediate one-time effect**, e.g., replay the Prefetch Buffer instructions
- **Immediate recurring effect**, e.g., incorrect order of the (replayed) instructions
- **Long-term effect**, e.g., corruption of the next branch target

➔ **Fault effects depend on the microarchitectural details and the execution context**

More details and other effects are described in the full paper

Robustness Analysis Results

Baseline CV32E40P + the most hardened VerifyPIN

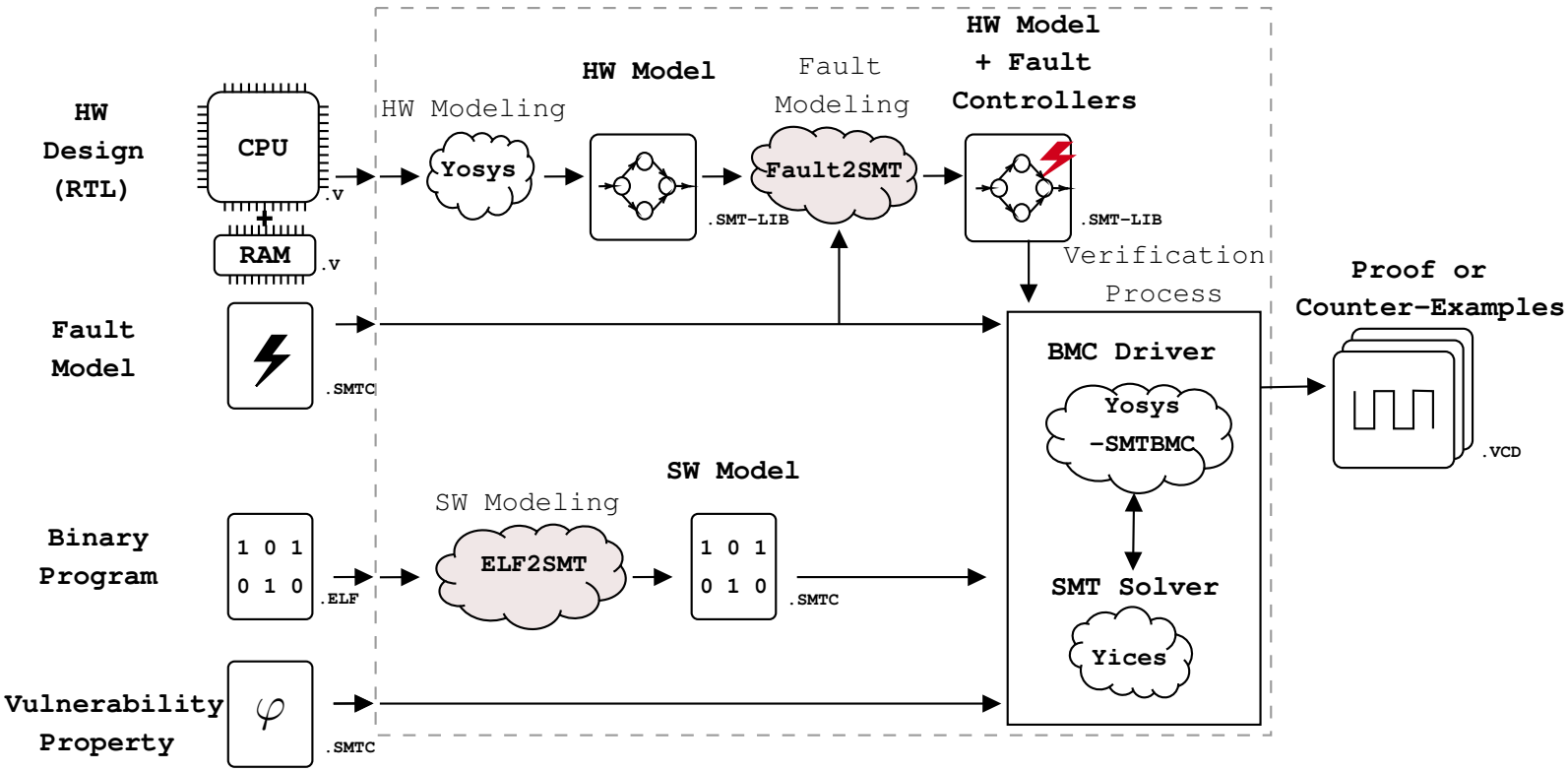
- No fault injection permits bypassing the secure authentication

Hardened CV32E40P + unprotected VerifyPIN

- No fault injection permits bypassing the secure authentication
- The hardware countermeasure is effective

More details and other effects are described in the full paper

Questions ?


HW Design (RTL)
CPU
.V
RAM
.V
HW Modeling
Yosys
HW Model
.SMT-LIB
Fault Modeling
Fault2SMT
HW Model + Fault Controllers
.SMT-LIB
Verification Process
Proof or Counter-Examples
.VCD
Fault Model
.SMTC
BMC Driver
Yosys -SMTBMC
SMT Solver
Yices
Binary Program
1 0 1
0 1 0
.ELF
SW Modeling
ELF2SMT
SW Model
1 0 1
0 1 0
.SMTC
Vulnerability Property
φ
.SMTC

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